AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1.-10 (Canceled)

11. (Currently Amended) A digital circuit for implementing a polynomial for estimating a fractional part of a logarithm of a number, the circuit comprising:

a function circuit for receiving an estimate of a fractional part and for generating a function of the estimate, wherein the function corresponds to an order of the polynomial;

a first constant multiplier for multiplying the estimate of a fractional part and a second polynomial coefficient and for generating a first output;

a second constant multiplier for multiplying the function of the estimate and a third polynomial coefficient and for generating a second output;

a first adder for adding the first output of the first constant multiplier and the second output of the second constant multiplier and for generating a first sum; and

a second adder for adding the first sum and a first polynomial coefficient and for generating an improved estimate of the fractional part;

wherein the order of the polynomial is greater than two.

12. (Canceled).

13. (Original) The digital circuit of 11, wherein the function circuit is a squaring circuit.

14. (Canceled).

15. (Currently Amended) A method for implementing a polynomial for estimating a fractional part of a logarithm of a number, the method comprising the steps of:

receiving an estimate of a fractional part;

generating a function of the estimate, wherein the function corresponds to an order of the polynomial;

multiplying the estimate of a fractional part and a second polynomial coefficient, wherein a first output is generated;

multiplying the function of the estimate and a third polynomial coefficient, wherein a second output is generated;

adding the first output of the first constant multiplier and the second output of the second constant multiplier, wherein a first sum is generated; and

adding the first sum and a first polynomial coefficient, wherein an improved estimate of the fractional part is generated;

wherein the order of the polynomial is greater than two.

16. (Canceled)

17. (Original) The method of claim 15, wherein the function circuit is a squaring circuit.

18.-20. (Canceled)

21. (Currently Amended) The ~~method~~ digital circuit of claim ~~8~~ 11, wherein the ~~steps are performed to calculate~~ digital circuit calculates one or more of signal to noise ratio, bit error rate, and power in dB.

22. (Original) The method of claim 15, wherein the steps are performed to calculate one or more of signal to noise ratio, bit error rate, and power in dB.

23.-27 (Canceled)

28. (Currently Amended) The ~~system~~ digital circuit of claim 11, wherein the ~~system~~ digital circuit is applied to one or more of ADSL, DSL, and G.SHDSL applications.

29. (Currently Amended) The ~~system~~ digital circuit of claim 28, wherein the ~~system~~ digital circuit is applied to one or more of central office, customer premise equipment, and wireless applications.